

Remarks

In the present response, eight claims (1-4, 7-8, 10, 12) are amended; one claim (9) is canceled; and eight claims (16-23) are newly added. Claims 1-8 and 10-23 are presented for examination.

I. Claim Rejections: 35 USC § 102

Claims 1-15 are rejected under 35 USC § 102(e) as being anticipated by USPN 6,134,710 (hereinafter Levine). This rejection is traversed.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Levine neither teaches nor suggests each element in claims 1-15, these claims are allowable over Levine.

Claim 1

Claim 1 recites numerous limitations that are not taught or suggested in Levine. By way of example, claim 1 recites hint code that includes a selected instruction to be removed from the set of object code. The claim also recites that the processor executes both the hint instruction and the selected instruction. Levine does not teach or suggest this limitation. Levine, in fact, teaches away from this limitation.

In Levine, the processor collects profile data “to determine where delays are occurring in the processing of the application program.” (Col. 6, lines 8-12). “An optimizing program then attempts to avoid or minimize the delays” (Col. 6, lines 20-21). The optimizing program then changes the object code:

The optimizing program then either **inserts changes to the object code** in real-time, or creates an **optimized change file that identifies object code changes** for the processing program for machine specific optimized performance. This optimized change file can then be used to **update the object code** of the processing program later, can be stored on a server for subsequent downloading to a processing program, or can be provided to a linker/loader program when **recompiling** the processing program. (Emphasis added: Col. 6, lines 32-41)

In contrast to Levine, claim 1 recites a selected instruction to be removed from the object code. The removed selected instruction is then executed (“execute both the hint instruction and the selected instruction”).

Claims 2-7 depend from claim 1. Thus, for at least the reasons given in connection with claim 1, claims 2-7 are also allowable over Levine.

Claim 8

Claim 8 recites numerous limitations that are not taught or suggested in Levine. By way of example, claim 8 recites an object code adapter that inserts a break instruction into the object code; the break instruction replaces a selected instruction in the object code. The claim further recites a processor that obtains and executes the removed selected instruction and then resumes execution of the object code. Levine does not teach or suggest this limitation. As noted in connection with claim 1, Levine, in fact, teaches away from the limitation of claim 8.

Claims 10-15 depend from claim 8. Thus, for at least the reasons given in connection with claim 8, claims 10-15 are also allowable over Levine.

II. New Claims

New claims 16-23 are added. No new matter is added. These claims contain numerous limitations that are not taught or suggested in the art of record. By way of example only, claim 16 recites “executing, by the processor, the hint code, wherein the hint code includes (i) a hint instruction, (ii) the selected instruction, and (iii) an instruction to resume execution of the object code.” These limitations are not taught or suggested in the art of record.

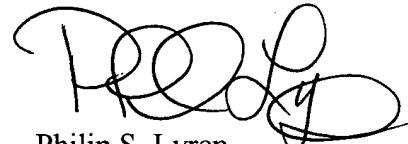
CONCLUSION

In view of the above, Applicants believe claims 1-8 and 10-23 are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. (281) 514-8236, Facsimile No. (281) 514-8332. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 15th day of October, 2004.

By Be Henry
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